REMARKS

The Office Action mailed November 26, 2001 has been reviewed and the comments of the Patent and Trademark Office have been considered. Claims 1-27 were pending in the application, with claims 12-14, 22 and 24 being withdrawn from consideration. Claims 1-11, 15-21, 23, and 25-27 are amended, new claims 28-31 are added and no claims have been cancelled. Therefore, claims 1-30 are pending in the application, with claims 1-11, 15-21, 23 and 25-31 submitted for reconsideration.

In the Office Action, claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,583,059 to Burghartz (hereafter "Burghartz"). Claims 5-11 and 15-27 are unpatentable over Burghartz and U.S. patent 5,241,214 to Herbots (hereafter "Herbots"). Applicants respectfully traverse these rejections for at least the following reasons.

Independent claims 1, 4, 11, 23, and 28 recite, *inter alia*, an IGFET (Insulated Gate Field Effect Transistor) in which an insulating film is located adjacent to a pair of main electrodes (the source and the drain). A gate electrode in contact with the insulating film comprises of (i) a first region composed of at least a first group IV element and a second group IV element, and (ii) a second region, formed on the first region, and comprising of the first group IV element.

Such a recited structure provides the advantage that the first region prevents leakage of boron (B) and promotes diffusion of arsenic (As). As a result, it is possible to prevent threshold voltages of the IGFET from varying. See, for example, last paragraph on page 30 of the specification (continuing onto page 31).

In sharp contrast, Burghartz describes a bipolar transistor that includes a buried oxide layer 2 of the SOI substrate, a p-SiGe base layer 5 on the buried oxide layer 2, and an n-emitter region 6 on the p-SiGe base layer 5. That is, Burghartz does not disclose or suggest the recited insulated gate electrode structure in an IGFET in which the recited first region is in contact with the insulating film located adjacent to the main electrodes.

In Fig. 2A of Burghartz, a region composed of one kind of a Group IV element (i.e., n-collector layer 4, and thin silicon film 3) is disposed between the buried oxide layer 2 and p-SiGe base layer 5. Therefore, Burghartz's structure does not provide the advantages of the

recited structure discussed earlier (prevents leakage of boron (B) and promotes diffusion of arsenic (As)).

Furthermore, Burghartz's disclosure describes a formation process for a bi-polar transistor, but does not describe a process for a MOS-FET in any detail. Therefore, there is no definitive disclosure regarding at which layer the p-SiGe base layer 5 of the bi-polar transistor is placed into the MOS-FET. Accordingly, the pending independent claims 1, 4, 11, 23, and 28 are believed to be fully patentable over the disclosure of Burghartz.

These deficiencies of Burghartz are not cured by Herbots. Specifically, Herbots discloses (referring to Fig. 1a-d) a wafer 12 (Si), an alloy layer 14 (SiGe) and an oxide layer 16 (SiGeO) formed one after another. The alloy layer 14 (SiGe) seems to be in contact with the oxide layer 16 (SiGeO). That is, Herbot's structure appears to be opposite (upside down) to that recited in the pending independent claims and, furthermore, does not provide the advantages of the recited structure discussed earlier herein.

Accordingly, neither Burghartz nor Herbots nor their reasonable combination teach or suggest the recited structure nor provide the advantages of the recited structure.

Independent claim 15 recites, *inter alia*, an epitaxial growth layer formed as an elevated part on the main electrodes wherein the growth layer comprises a first region and a second region of a first conductivity type that are formed in contact with a semiconductor region of the same first conductivity type. In sharp contrast, Burghartz discloses (with reference to Fig. 2A) a n-collector region (Si), p SiGe base layer 5 (SiGe) and a n-emitter region 6 (Si) that are stacked over each other. That is, the bi-polar transistor in Burghartz has the n-p-n structure. Therefore, Burghartz does not disclose the recited structure in claim 15.

As discussed earlier, the first (SiGe) region in the elevated part prevents impurities, for example, Boron from leaking into the semiconductor region. Therefore, this advantage of the structure recited in claim 15 is not achievable by structure disclosed in Burghartz. Nor are these deficiencies cured by Herbots. Accordingly, claim 15 is believed to be patentable over the applied prior art.

The dependent claims are also in condition for allowance for at least the same reasons stated above as the independent claims on which they ultimately depend. In addition, they recite additional patentable features when considered as a whole.

In view of the foregoing, applicants believe that the application is in condition for allowance. An early notice to this effect is earnestly solicited. If there are any questions regarding the application or if an examiner's amendment would facilitate the allowance of one or more of the claims, the examiner is invited to contact the undersigned attorney at the local telephone number below.

Respectfully submitted,

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February 26, 2002
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Attached: Attachment A

Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge deposit account No. 19-0741 for any such fees; and applicants hereby petition for any needed extension of time.

ATTACHMENT A

Marked up version of claim amendments made in the Amendment filed February 26, 2002

1. (Amended) A semiconductor [integrated circuit including an insulated gate field effect transistor of which gate electrode] device comprising:

a pair of main electrodes used as source and drain electrodes;

an insulating gate film adjacent to the pair of main electrodes; and

a gate electrode comprising a first region composed of at least a first [IV] group IV element and a second [IV] group IV element [which are different from each other,] and formed [on an] in contact with the insulating [insulated] gate film [on a semiconductor substrate; and (b)], and a second region composed of the first [IV] group IV element and formed on the first region.

2. (Amended) The semiconductor [integrated circuit] device of claim 1, wherein the first region of the gate electrode has a composition ratio of the second [IV] group IV element gradually reduced in accordance with a distance from the [insulated] insulating gate film.

3. (Amended) The semiconductor [integrated circuit] device of claim 1, wherein the first region of the gate electrode has a composition ratio of the second [IV] group IV element stepwise reduced in accordance with a distance from the [insulated] insulating gate film.

4. (Amended) A semiconductor [integrated circuit] device comprising:

[(a)] an insulated gate field effect transistor [including] comprising a pair of main electrodes used as a source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode [which is provided with] comprising a first region composed of at least a first [IV] group IV element and a second [IV] group IV element [which are different from each other] and formed [on an] in contact with the insulating

[insulated] gate film [on a semiconductor substrate], and a second region composed of the first [IV] group IV element and formed on the first region; and

[(b)] a silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second [IV] group IV element.

5. (Amended) The semiconductor [integrated circuit] device of claim 4, wherein the first [IV] group IV element of the gate electrode is Si (silicon), the second [IV] group IV element of the gate electrode is Ge (germanium), and the silicide electrode is composed of a $CoSi_y$, or $TiSi_y$ layer which is substantially free from Ge.

6. (Amended) The semiconductor [integrated circuit] device of claim 5, wherein the first region of the gate electrode has a thickness larger than a width of a depletion layer of the gate electrode composed of Si.

7. (Amended) The semiconductor [integrated circuit] device of claim 6, wherein a composition ratio of Ge of the first region of the gate electrode is at least 0.1 or larger.

8. (Amended) The semiconductor [integrated circuit] device of claim 7, wherein the gate electrode contains at least B (boron).

9. (Amended) The semiconductor [integrated circuit] device of claim 7, wherein the gate electrode contains at least As (arsenic).

10. (Amended) The semiconductor [integrated circuit] device of claim 4, wherein the first [IV] group IV element of the gate electrode is Si, the second [IV] group IV element of the gate electrode is C (carbon), and the silicide electrode is composed of a $CoSi_y$, or $TiSi_y$ layer which is substantially free of C.

11. (Amended) A semiconductor [integrated circuit] device comprising:

[(a)] an insulated gate field effect transistor [including] having a pair of main electrodes used as source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode [which is provided with] comprising a first region composed of at least a first [IV] group IV element and a second [IV] group IV element

[which are different from each other] and formed [on an] in contact with the insulating [insulated] gate film [on a semiconductor substrate], and a second region composed of a multiple element compound including at least the first and second [IV] group IV elements and metal, and formed on the first region; and

[(b)] a silicide electrode formed in contact with the second region of the gate electrode, composed of the first [IV] group IV element and metal, and being substantially free from the second [IV] group IV element.

15. (Amended) A semiconductor [integrated circuit] device comprising:

[(a)] a semiconductor region of a first [conductive] conductivity type;

[(b)] an epitaxial growth layer formed on the semiconductor region and [including] having a first region of the first conductivity type composed of at least a first [IV] group IV element and a second [IV] group IV element [which are different from each other] and formed in contact with the semiconductor region and a second region of the first conductivity type composed of the first [IV] group IV element and formed in contact with the first region; and

[(c)] a silicide electrode formed on the second region of the epitaxial growth layer.

16. (Amended) The semiconductor [integrated circuit] device of claim 15, wherein the semiconductor region is a source or drain electrode of the insulated gate field effect transistor, and the epitaxial growth layer is an elevated source or drain electrode.

17. (Amended) The semiconductor [integrated circuit] device of claim 16, wherein the first [IV] group IV element of the elevated source or drain electrode is Si, the second [IV] group IV element of the elevated source or drain electrode is Ge, and the silicide electrode is made of a $CoSi_y$ or $TiSi_y$ layer which is substantially free from Ge.

18. (Amended) The semiconductor [integrated circuit] device of claim 17, wherein a composition ratio of Ge in the first region of the elevated source or drain electrode is at least 0.1 or more, and a thickness of the first region is at least 2nm from the semiconductor region.

19. (Amended) The semiconductor [integrated circuit] device of claim 18, wherein the elevated source or drain electrode contains at least B.

20. (Amended) The semiconductor [integrated circuit] device of claim 18, wherein the elevated source or drain electrode contains at least As.

21. (Amended) The semiconductor [integrated circuit] device of claim 16, wherein the first [IV] group IV element of the elevated source or drain electrode is Si, the second [IV] group IV element of the elevated source or drain electrode is C, and the silicide electrode made of a $CoSi_y$ or $TiSi_y$ layer which is substantially free from C.

23. (Amended) A semiconductor [integrated circuit] device comprising:

[(a)] an insulated gate field effect transistor [including] having a pair of main electrodes used as source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode [provided with] comprising a first region [which is] composed of at least a first [IV] group IV element and a second [IV] group IV element [of different kinds] and formed [on an] in contact with the insulating [insulated] gate film [of a semiconductor substrate], and a second region [which is] composed of the first [IV] group IV element and formed on the first region [, and a main electrode];

[(b) an] a respective elevated electrode formed on the main [electrode] electrodes, and having a third region composed of a third [IV] group IV element and a fourth [IV] group IV element [which are different from each other] and a fourth region formed on the third region and composed of the third [IV] group IV element;

[(c)] a first silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second [IV] group IV element; and

[(d)] a second silicide electrode formed in contact with the fourth region of the elevated electrode, and being substantially free from the fourth [IV] group IV element.

25. (Amended) The semiconductor [integrated circuit] device of claim 1, wherein a layer is added between the [insulated] insulating gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first [IV] group IV element or the second [IV] group IV element.

26. (Amended) The semiconductor [integrated circuit] device of claim 4, wherein a layer is added between the [insulated] insulating gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first [IV] group IV element or the second [IV] group IV element.

27. (Amended) The semiconductor [integrated circuit] device of claim 11, wherein a layer is added between the [insulated] insulating gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first [IV] group IV element or the second [IV] group IV element.